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PERFORMANCE ANALYSIS OF DIFFERENT N-BIT ADDERS USING REVERSIBLE LOGIC ON FPGA BOARD USING CHIPSCOPE

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ABSTRACT

In current scenario, high-performance chips releasing large amounts of heat impose practical limitation. Reversible circuits that conserve information, by uncomputing bits instead of throwing them away. Reversible logic design attracting more interest due to its low power consumption. The paper gives brief idea to build variety of n-bit adders like Ripple carry adder, Carry look ahead adder, Carry save adder, Carry skip adder and Carry select adder circuits using the basic reversible gate like Peres gate, TSG, MTS, Taffoli, HNG etc. The designed adders are verified using chipscope on FPGA platform and compared w.r.t quantum cost, ancilla input, number of gates used and garbage outputs. Among these ripple carry adder and carry look ahead adder are efficient interms of garbage output and number of gates used. These adders can be used to build more complex circuits like ALU design.

KEYWORDS: Reversible logic, quantum cost, ancilla, garbage, ripple carry, carry look ahead, carry select, carry save, carry skip adder.

I. INTRODUCTION

Irreversible hardware computation results in energy dissipation due to information loss. According to Landaue's research, the amount of energy dissipated for every irreversible bit operation is at least KTln(2) joules, where k is the Boltzmann's constant and T is the temperature at which operation is performed, where $K=1.3806505*10^{-23}m^2kg^{-2}k^{-1}$.

The heat generated due to the loss of one bit of information is very small at room temperature but when the number of bits is more as in the case of high speed computational works the heat dissipated by them will be so large that it affects the performance and results in the reduction of lifetime of the components.

II. BASIC REVERSIBLE LOGIC GATES

Reversible logic has received great attention in the recent years due to their ability to reduce the power dissipation which is the main requirement in low power VLSI design. It has wide applications in low power CMOS and Optical information processing, DNA computing, quantum computation and nanotechnology. In 1973, Bennett showed that KTln(2) energy would not dissipate from a system as long as the system allows the reproduction of the inputs from observed outputs[1].

Reversible logic supports the process of running the system both forward and backward. This means that reversible computations can generate inputs from outputs and can stop and go back to any point in the computation history.

Basic definition

A circuit is said to be reversible if input and output vector can be uniquely recovered and there is a one-to-one correspondence between their assignments i.e. not only the outputs can be uniquely determined from the inputs, but also the inputs can be recovered from the outputs, Energy dissipation can be reduced or even eliminated if computation becomes information-lossless

Peres gate

Peres is 3*3 matrix, its input vector is I(A, B, C) and the output vector is O(P, Q, R). Quantum cost of a Peres gate is 4. In the proposed design Peres gate is used because of its lowest quantum cost[1].

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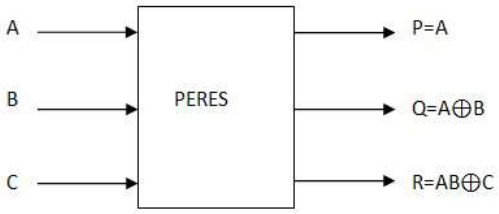

Figure 1. Peres gate

Table 1. Truth table of Peres gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Taffoli gate

It is a 3*3 Toffoli gate. The input vector is I (A, B, C) and the output vector is O(P,Q,R). Quantum cost of a Toffoli gate is 5[1]**.**

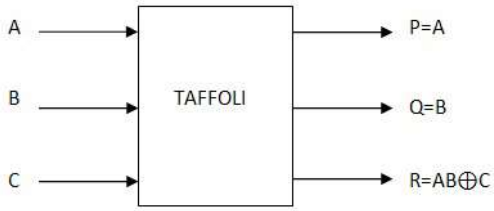

Figure 2. Taffoli gate

Table 2. Truth table of Taffoli gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

TSG gate

The input vector is I(A,B, C, D) and the output vector is O(P, Q, R, S)[1]. Quantum cost of a TSG gate is 4. The TSG gate is capable of implementing all Boolean functions and can also work singly as a reversible full adder.

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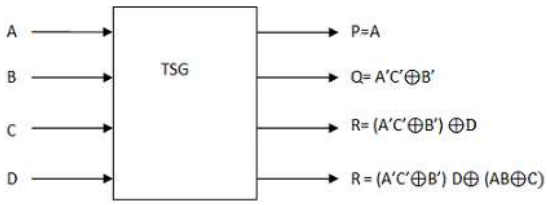

Figure 3. TSG gate

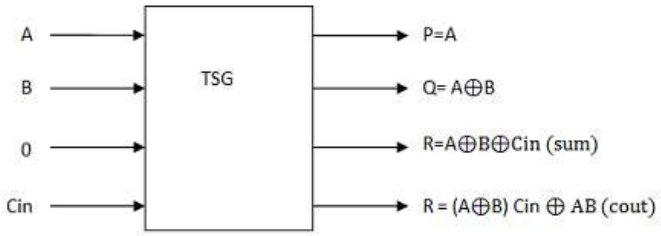

Figure 4. TSG gate as a full adder

MIG gate

A 4*4 reversible gate Modified Islam Gate(MIG) is already had proposed shown in fig. 5. In this gate the input vector is given by A,B,C,D and output vector is given by P,Q,R,S. The cost is 7[7].

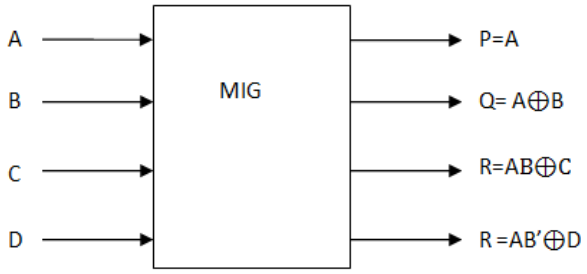

Figure 5. MIG gate

HNG gate

It is 4*4 matrix. The reversible HNG gate can work singly as a reversible full adder. If the input vector I = (A, B, Cin, 0), then the output vector is O = (P=A, Q=Cin, R=Sum, S=Cout) and its cost is 6[2].

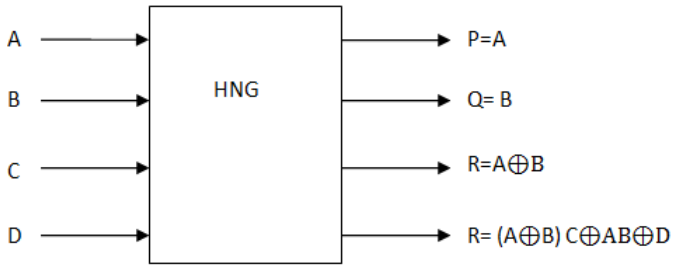

Figure 6. HNG gate

MTS gate

The MTSG gate is with 4*4 matrix input vector (A, B ,C, D) and output vector(P, Q, R, S). The quantum cost of MTS is 6[2].

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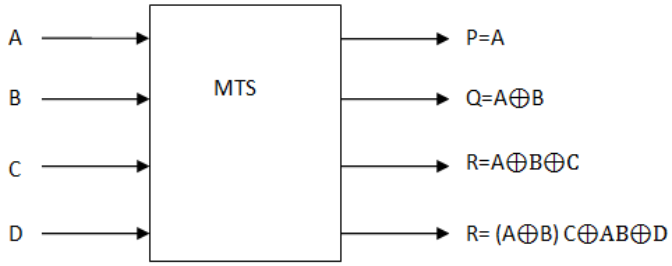

Figure 7. MTS gate

DPG gate

It is a 4*4 Double Peres Gate. The input vector is I(A,B,C,D) and the output vector is O(P,Q,R,S) Its quantum cost is 6[2].

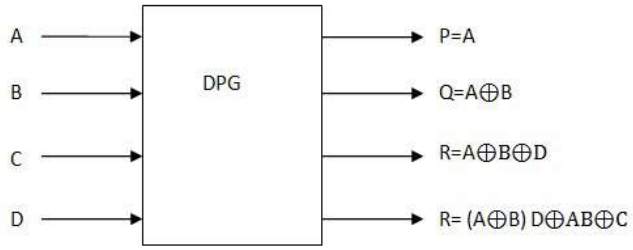

Figure 8. DPG gate

TKS gate

The TKS gate can be used to implement any Boolean function since two of its outputs (P & R) can function as 2:1 multiplexer. Its equations are as shown fig 9. It is 3*3 matrix[2].

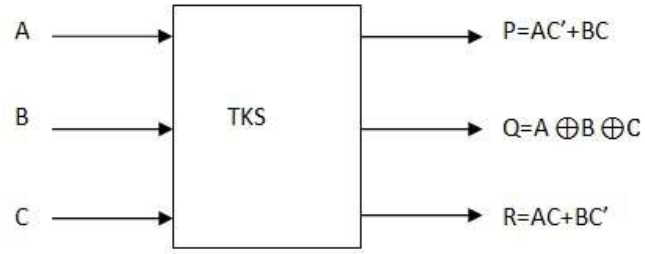

Figure 9. TKS gate

III. PROPOSED DESIGN OF ADDERS

An adder is a digital circuit that performs addition of numbers. In many computers and other kinds of processors adders are used in the arithmetic logic units. They are also utilized in other parts of the processor, where they are used to calculate addresses, table indices, increment and decrement operators, and similar operations.

Digital Adder is a digital device capable of adding two digital n-bit binary numbers, where n depends on the circuit implementation. Digital adder adds two binary numbers A and B to produce a sum S and a carry C. The variety of adders are ripple carry adder, carry look ahead adder, carry select, carry save, carry skip adder and the same are designed in this paper.

Ripple carry adder

Multiple full adder circuits can be cascaded in parallel to add an N-bit number[6]. For an N- bit parallel adder, there must be N number of full adder circuits. A ripple carry adder is a logic circuit in which the carry-out

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of each full adder is the carry in of the succeeding next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage.

This adder can be implemented using Peres, TSG, HNG, MTS and DPG. The best is with using MTS as it has less number of gates, garbage, ancilla and quantum cost as shown in table III.

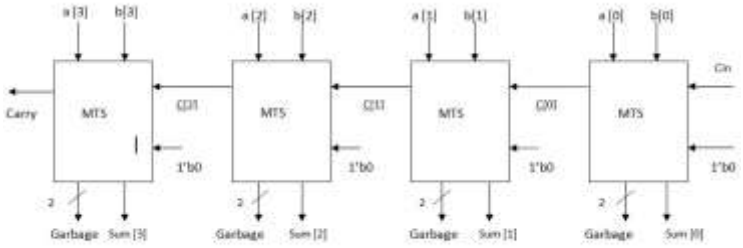

Figure 10. Ripple carry adder

Table III. Analysis of ripple carry adder

Gates used	No of gates	Garbage	Ancilla	Quantum cost
Fredkin[6]	9	8	4	45
Peres	8	8	4	32
TSG	4	8	4	40
HNG	4	8	4	24
MTS	4	8	4	24
DPG	4	8	4	24

Carry look ahead adder

A carry-lookahead adder (CLA) or fast adder is a type of adder used in digital logic. A carry-lookahead adder improves speed by reducing the amount of time required to determine carry bits. It can be contrasted with the simpler, but usually slower, ripple carry adder for which the carry bit is calculated along side the sum bit, and each bit must wait until the previous carry has been calculated to begin calculating its own result and carry bits. The carry-lookahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits[6].

Peres or MIG are used to produce propogator and generator required as input for carry look ahead adder. This adder can be implemented using only Peres along with either peres or MIG. The best is using Peres for producing propogator and generator and the same Peres for producing sum and carry refer fig. 11, as it has less number of gates, garbage, ancilla and quantum cost as shown it table IV.

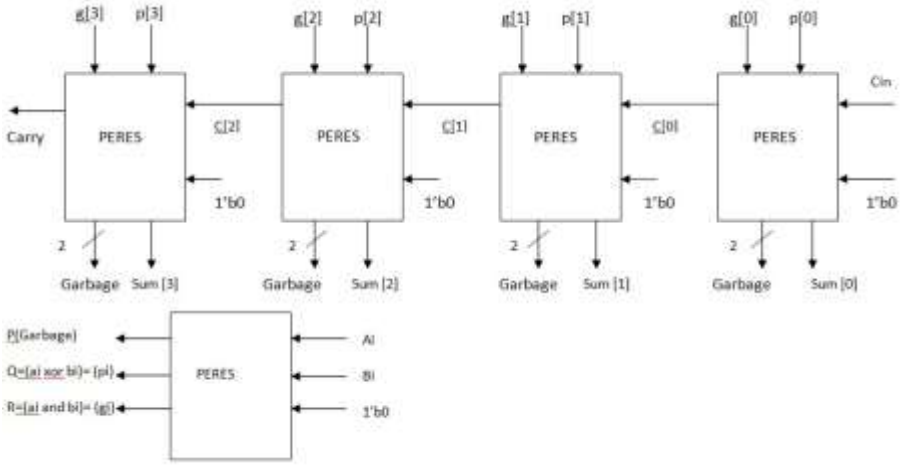

Figure 11. Carry look ahead adder

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Table IV. Analysis of carry look ahead adder

Gates used	No of gates	Garbage	Ancilla	Quantum cost
Fredkin[6]	20	24	24	56
Peres	8	8	4	32
Peres and MIG	8	12	8	44

Carry select adder

The carry-select adder generally consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders). In order to perform the calculation twice, one time assuming carry-in as zero and the other time assuming carry as one. After the two results are calculated, the correct sum, as well as the correct carry-out, is then selected with the multiplexer when the correct carry-in is known.

The fig. 12 is the basic building block of a carry-select adder. Two 4-bit ripple carry adders are multiplexed together, where the resulting carry and sum bits are selected by the carry-in. Since one ripple carry adder assumes a carry-in of 0, and the other assumes a carry-in of 1, selecting which adder had the correct assumption via the actual carry-in yields the desired result.

This adder can be implemented using Peres, TSG, HNG, MTS, DPG along with TKS, because TKS can be implemented as MUX. The best is with using MTS as it has less number of gates, garbage, ancilla and quantum cost as shown in table V.

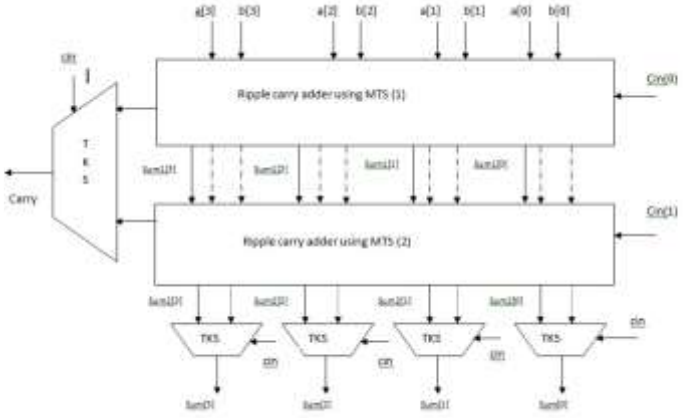

Figure 12. Carry select adder

Table V. Analysis of Carry select adder

Gates used	No of gates	Garbage	Ancilla	Quantum cost
Peres and TKS	21	26	8	64 +QC of TKS
TSG and TKS	13	26	8	80+QC of TKS
HNG and TKS	13	26	8	48+QC of TKS
MTS and TKS	13	26	8	48+QC of TKS
DPG and TKS	13	26	8	48+QC of TKS

Carry skip adder

A carry-skip adder (also known as a carry-bypass adder) is an adder implementation that improves on the delay of a ripple-carry adder with little effort compared to other adders. The improvement of the worst-case delay is achieved by using several carry-skip adders to form a block-carry-skip adder.

The n-bit-carry-skip adder consists of a n-bit-carry-ripple-chain, a n-input AND-gate and one multiplexer. Each propagate bit pi, that is provided by the carry-ripple-chain is connected to the n-input AND-gate. The

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resulting bit is used as the select bit of a multiplexer that switches either the last carry-bit c[n] or the carry-in c[0] to the carry-out signal cout.

This adder can be implemented using MTS, DPG, Taffoli along with TKS, because TKS can be implemented as MUX. The best is with using MTS and taffoli as it has less number of gates, garbage, ancilla and quantum cost as shown in table VI.

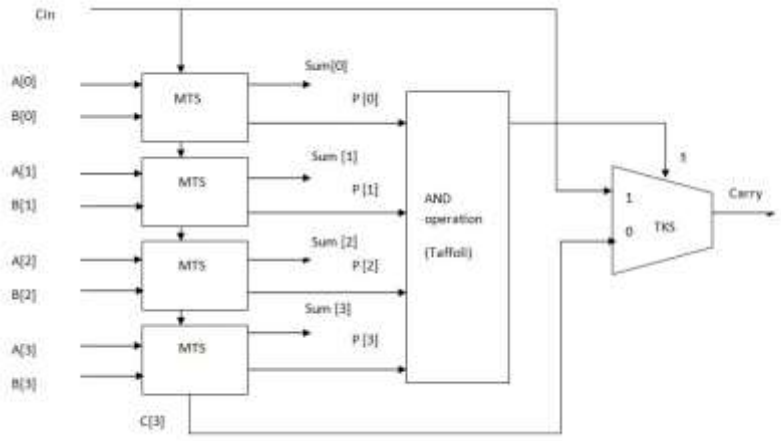

Figure 13. Carry skip adder

Table VI. Analysis of carry skip adder

Gates used	No of gates	Garbage	Ancilla	Quantum cost
R and NFA[6]	10	13	10	52
MTS, taffoli and TKS	8	12	7	39 +QC of TKS
DPG, taffoli and TKS	8	12	7	39 +QC of TKS

Carry save adder

A carry-save adder is a type of digital adder, used in computer micro architecture to compute the sum of three or more n-bit numbers in binary. It differs from other digital adders in that it outputs two numbers of the same dimensions as the inputs, one which is a sequence of partial sum bits and another which is a sequence of carry bits.

This adder can be implemented using Peres, MIG, TSG, HNG. The best is with using peres and HNG as it has less number of gates, garbage, ancilla and quantum cost as shown in table VII.

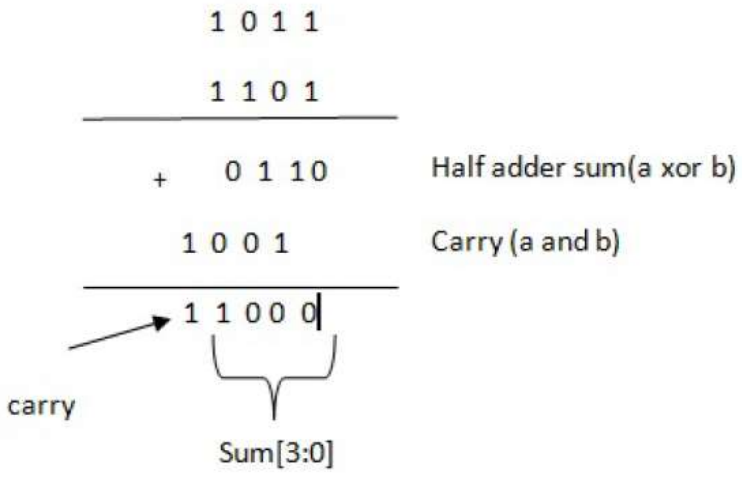

Figure 14. Carry save adder

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Table VII. Analysis of carry save adder

Gates used	No of gates	Garbage	Ancilla	Quantum cost
MTG and peres	14	19	11	68
TSG and peres	9	15	11	66
TSG and MIG	9	19	15	78
HNG and peres	9	15	11	46
MIG and HNG	9	19	15	58

Summary of adders

The best design from each of the adder is considered and compared among different types of adders. From fig. VIII ripple carry adder and carry look ahead adder are efficient interms of garbage output and number of gates used.

Table VIII. Summary of adders designed

Adder	Gates used	No of gates	Garbage	Ancilla	Quantum cost
Ripple carry	MTS	4	8	4	24
Carry look ahead	Peres, peres	8	8	4	32
Carry select	MTS,TK	13	26	8	48+QC of TKS
Carry skip	MTS, Taffoli, TKS	8	12	7	39 +QC of TKS
Carry save	Peres, HNG	9	15	11	46

IV. SIMULATION RESULTS

Xilinx is used for implementing designed adders, chipscope is platform to analyze waveforms or outputs. It is a design which is fully simulated and requires board level testing. JTAG interface acts like communicator between FPGA and PC. Xilinx ISE offers analysis tools for both design implementation and design concept. The ISE tools help to reach optimal design results with timing predictability and reconfiguration with greater flexibility and size.

Ripple carry adder output

Here inputs A and B are of 4 bit and a cin. Output sum is of 4 bit and a carry. Inputs are taken as cin 1, a as 1111 and b as 1111, referring fig. 15, output obtained sum and carry as 1111(F in hex) and 1 respectively are verified.

Carry select adder output

Here inputs A and B are of 8 bit and a cin. Output sum is of 8 bit and a carry .Inputs are taken as cin 1, a as 11111111 and b as 11111111, referring fig. 16, output obtained sum and carry as 11111111(FF in hex) and 1 respectively are verified.

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Carry skip adder output

Here inputs A and B are of 32 bit and a cin. Output sum is of 32 bit and a carry. Inputs are taken as cin 1, a as FFFFFFFF and b as 00003FFF, referring fig. 17, output obtained sum and carry as 00003FFF and 1 respectively are verified.

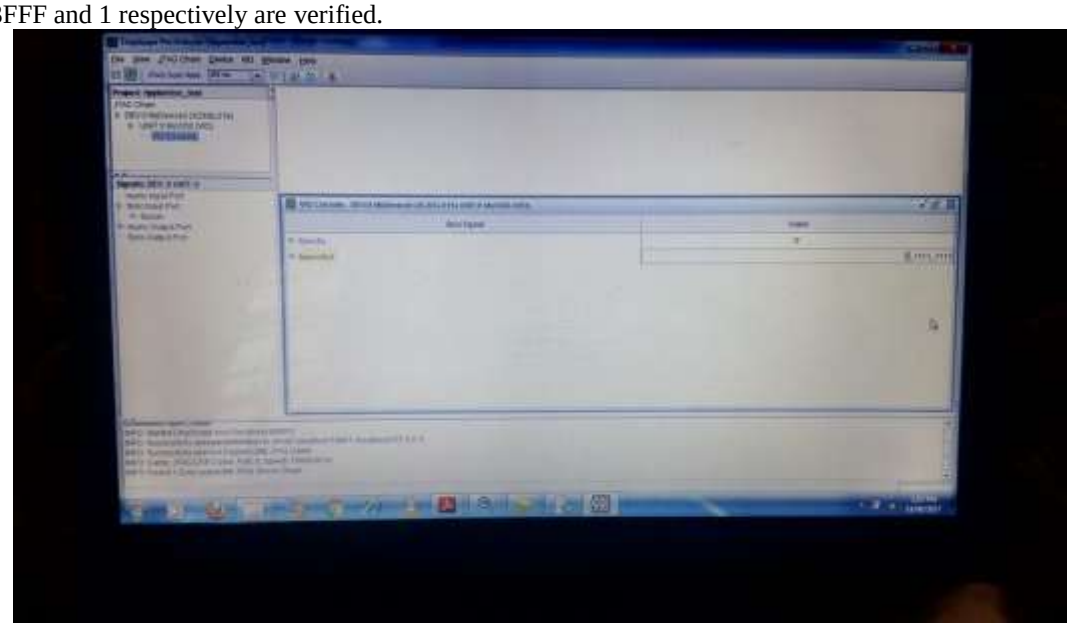

Figure 15. Result of ripple carry adder

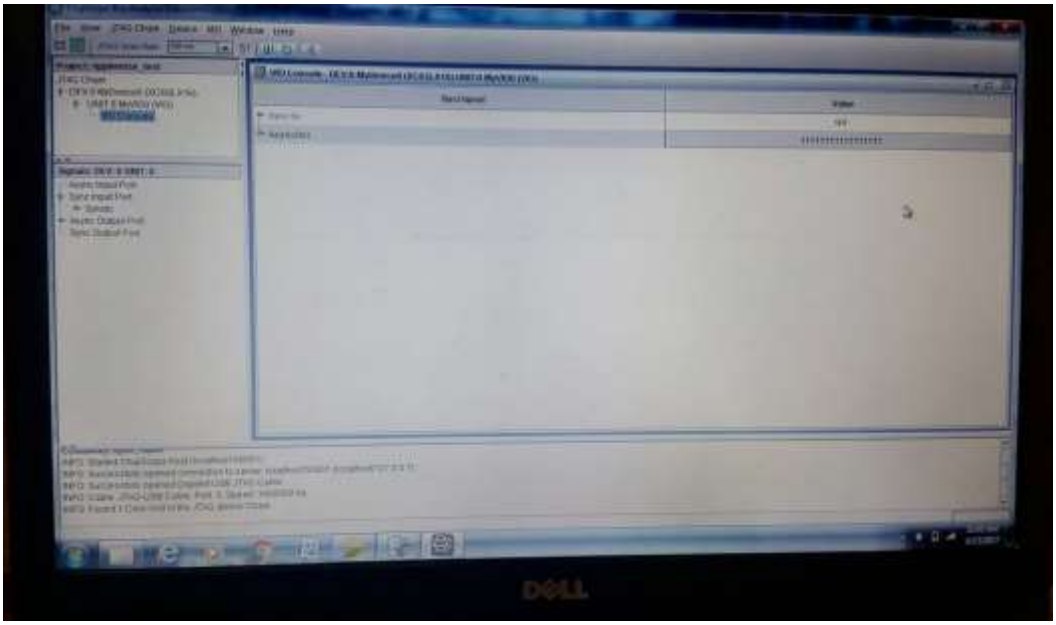

Figure 16. Result of carry select adder

Carry save adder output

Here inputs A and B are of 16 bit and a cin. Output sum is of 16 bit and a carry. Inputs are taken as cin 1, a as 1111111111111111 and b as 1111111111111111, referring fig. 18, output obtained sum and carry as 1111111111111111(FFFF in hex) and 1 respectively are verified.

Carry look ahead adder output

Here inputs A and B are of 16 bit and a cin. Output sum is of 16 bit and a carry. Inputs are taken as cin 0, a as 0000000000000000 and b as 1111111111111111, referring fig. 19, output obtained sum and carry as 1111111111111111(FFFF in hex) and 0 respectively are verified.

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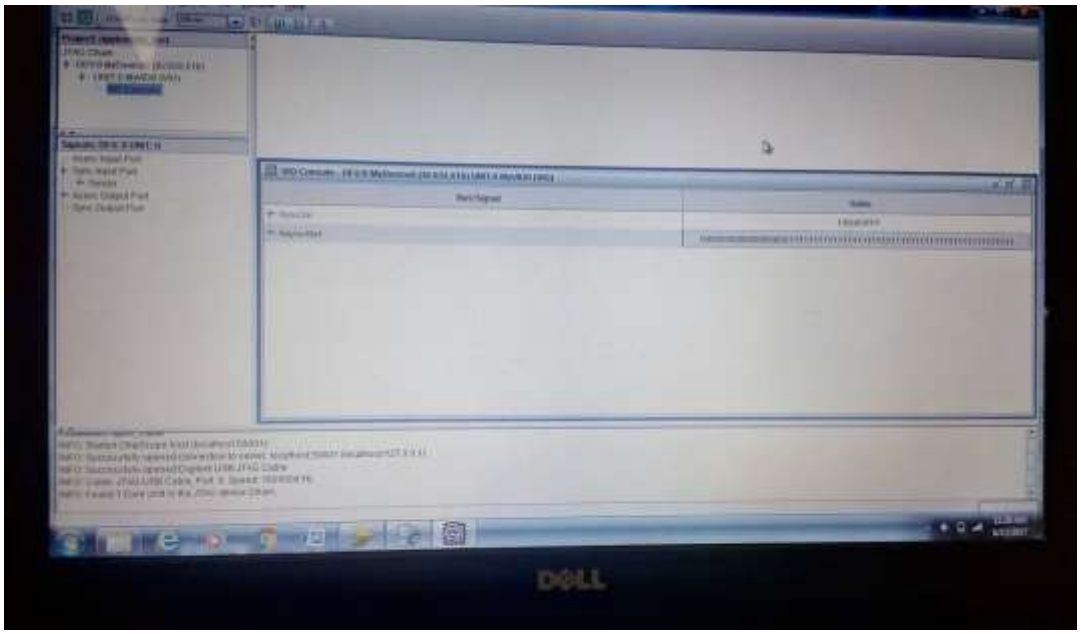

Figure. 17. Result of carry skip adder

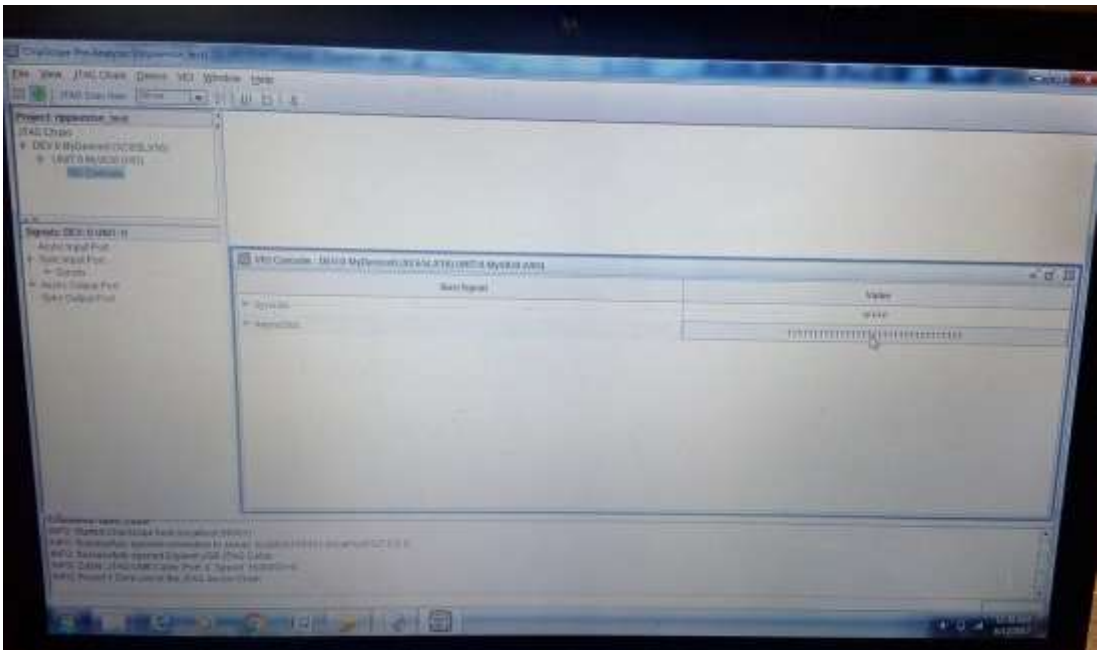

Figure 18. Result of carry save adder

V. APPLICATIONS

Reversible computing may have applications in computer security and transaction processing, but the main long-term benefit will be felt very well in those areas which require high energy efficiency, speed and performance. It include the area like

1. Low power CMOS- Reversible logic can be used in design of low power circuits.
2. Quantum computer- A new developing era of computers make use of this logic as basics in its processing unit.
3. Nanotechnology- Reversible gate may be used to produce any logic operation. It is possible to find physical representations for the information, so that when processed with reversible logic, the energy of the output is equal to the energy of the input.

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4. Optical computing- Reversible nonlinear interface devices have a picoseconds response time and hence produce a very fast half-adder circuit. These devices can be used in the implementation of an optical CPU.
5. Design of low power arithmetic and data path for digital signal processing(DSP).
6. Field Programmable Gate Arrays (FPGAs) in CMOS technology for extremely low power, high testability and self-repair.

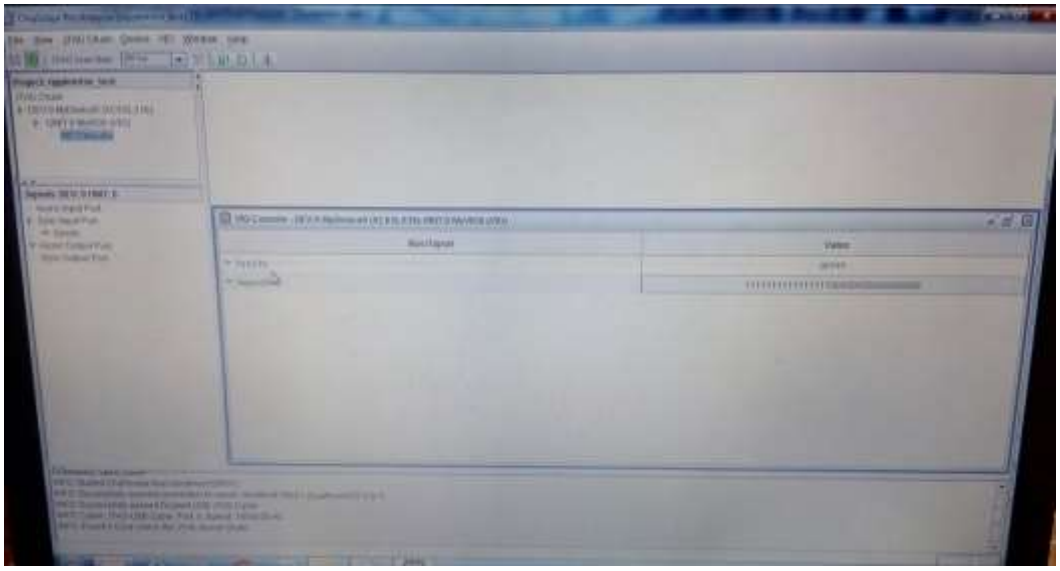

Figure 19. Result of carry look ahead adder

VI. ADVANTAGES

1. Information, like energy, is conserved under the laws of physics.
2. Thermodynamics can be used to tie the irreversibility of a system to the amount of heat it dissipates.
3. An energy-lossless circuit must therefore be information lossless.
4. Furthermore, there is evidence to suggest that reversible circuits may be built in an energy-lossless way.
5. Reversible computing are used in computer for security and transaction processing.

VII. CONCLUSION AND FUTURE SCOPE

Reversible logic design attracting more interest due to its low power consumption. The paper gives brief idea to build variety of n-bit adders like Ripple carry adder, Carry look ahead adder, Carry save adder, Carry skip adder and Carry select adder circuits using the basic reversible gate like Peres gate, TSG, MTS, Taffoli, HNG etc. The designed adders are verified using chipscope on FPGA platform and compared w.r.t quantum cost, ancilla input, number of gates used and garbage outputs. Among these ripple carry adder and carry look ahead adder are efficient interms of garbage output and number of gates used. These adders can be used to build more complex circuits like ALU design.

VIII. ACKNOWLEDGEMENTS

The sense of contentment and elation that accompanies the successful completion of the project and its paper would be incomplete without mentioning the names of the people who helped in accomplishing this.

We take this opportunity to thank our vice chancellor Dr.Ashok Shettar, for providing healthy environment in the college, which helped in concentrating on the task.

We express a deep sense of gratitude to our H.O.D. Dr.Priyatam Kumar, for providing the inspiration required for taking the project to its completion and for their inspiring guidance and promising support they gave during the completion of project.

Last but not the least we would like to thank all the staff members, teaching and nonteaching staff for helping us during the course of the project and paper publishing .

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CODEN: IJESS7

IX. REFERENCES

[1] P. .R.Yelekar and P. S. S. Chiwande, "Introduction to reversible logic gates its application," National Conference on Information and Communication Technology., vol. 04, No 1, Jan 2015.
[2] A. K. Raghava Garipelly, P.Madhu Kiran, "A review on reversible logic gates and their implementation a review on reversible logic gates and their implementation" International Journal of Emerging Technology and Advanced Engineering., vol. 03, No 03, March 2013.
[3] A. A. Pallav Gupta and N. K., "An algorithm for synthesis of reversible logic circuits" IEEE Transaction On Computer- Aided Design Of Integrated Circuits And Systems,, vol. 25, No 11, March 2014.
[4] H. R. B. Nagamani A N, Jayashree H V, "Novel low power comparator design using reversible logic gates" Indian Jour nal of Computer Science and Engineering., vol. 02, No 04, Nov 2011.
[5] M. H.R.Bhagyalakshmi, "Optimized reversible bcd adder using new reversible logic gates" Indian Journal of Computer Science and Engineering., vol. 02, No 02, Feb 2012.
[6] P. C. P. K. LALA, J.P. PARKERSON, "Adder designs using reversible logic gates" Wseas transactions on circuits and system, vol. 09 No 06, Jun 2014.
[7] Girija S, Raghavendra G R, Manjushree B R, Nirmalraj R, Prakruthi U S "Design of Carry Look-Ahead Adder Using Reversible Logic Gates" International Journal of Electrical, Electronics and Computer Systems,vol.02 No 04 ,Dec 2014.
[8] Naman Sharma, Upanshu Saraswat, Rajat Sachdeva "Implementation of a Carry Look-Ahead Adder circuit using Reversible Logic" International Journal of Scientific & Engineering Research,vol.06, Issue 10, Oct- 2015. .
[9] Vandana Shukla, O. P. Singh, G. R. Mishra, R. K. Tiwari "Novel Design of A 4:1 Multiplexer Circuit Using Reversible Logic" International Journal of Computational Engineering Research,vol.03, Issue 10, Oct- 2013.
[10] M.Bharathi, K.Neelima "scope of reversible engineering at gate-level: fault-tolerant combinational adders" International Journal of VLSI design & Communication Systems (VLSICS),vol.03, No 02 , Apr 2012.
[11] B.Raghu kanth, B.Murali Krishna, M. Sridhar, V.G. Santhi Swaroop "A distinguish between reversible and conventional logic gates" International Journal of Engineering Research and Applications (IJERA),Vol.02, Issue 2, Mar-Apr 2012.
[12] Tabrez Anjum, Shrikant Ahirwar "Verilog HDL Implementation of Squarer Using Reversible Logic Gates" International Journal & Magazine of Engineering, Technology, Management and Research,vol.02, Issue 09, sep 2015.

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